Fast Big-Integer Arithmetic on SVP64 at up to 256-bits/cycle and beyond

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FOSDEM 2024

libreSOC

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sv.add *r3, *r15, r12  # adds 3 times
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# expands to:
add r3, r15, r12  # no * means r12 doesn't increment
add r4, r16, r12  # * means r3 and r15 increment
add r5, r17, r12
```

Big-Integer Addition on SVP64

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```
setvl 0, 0, 4, 0, 1, 1 # makes stuff run 4 times
addic r0, r0, 0  # clear CA (carry flag)
sv.adde *r4, *r4, *r8  # carry-propagating add
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# expands to:
addic r0, r0, 0  # clear CA (carry flag)
adde r4, r4, r8
adde r5, r5, r9
adde r6, r6, r10
adde r7, r7, r11
```

Big-Integer Addition on SVP64

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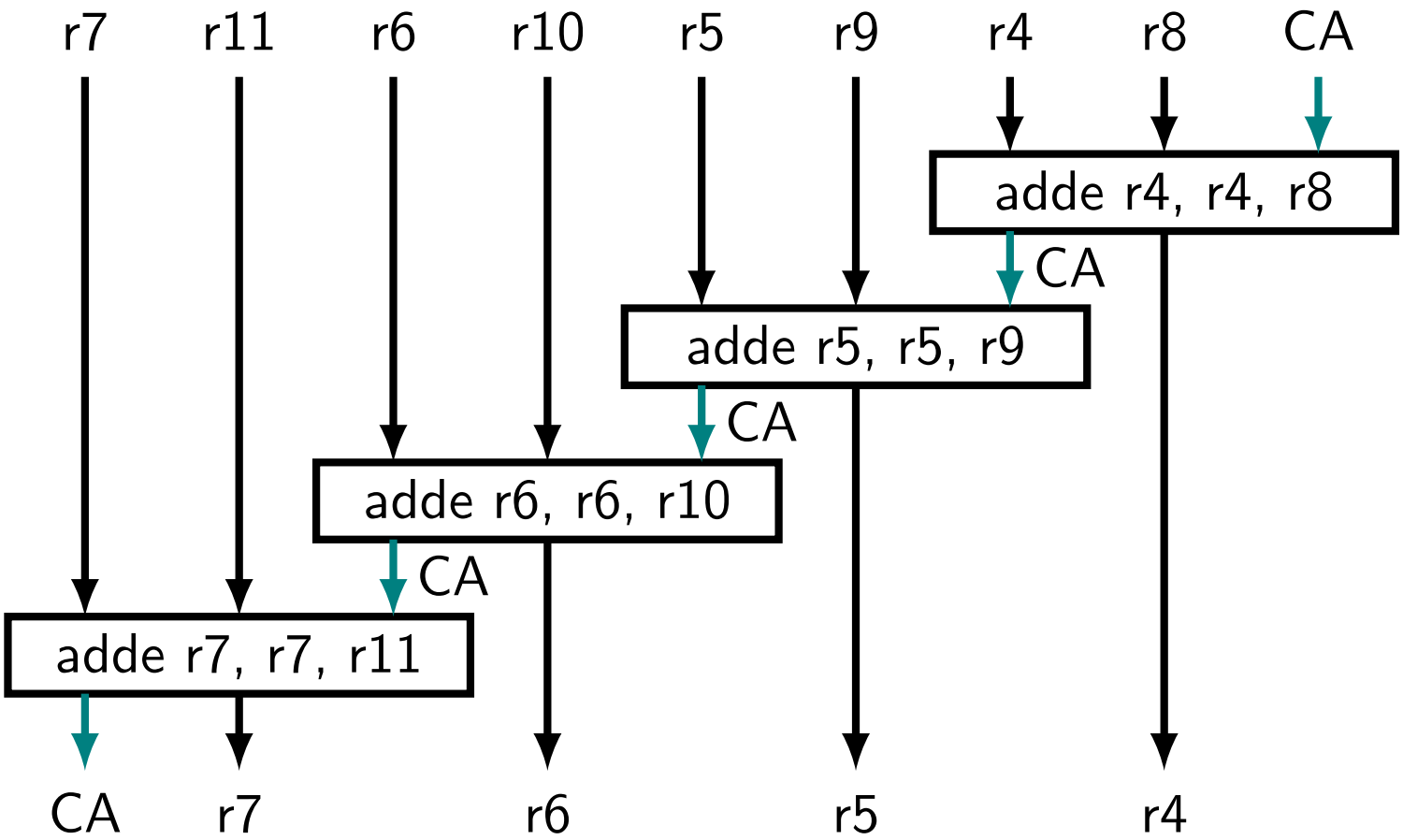
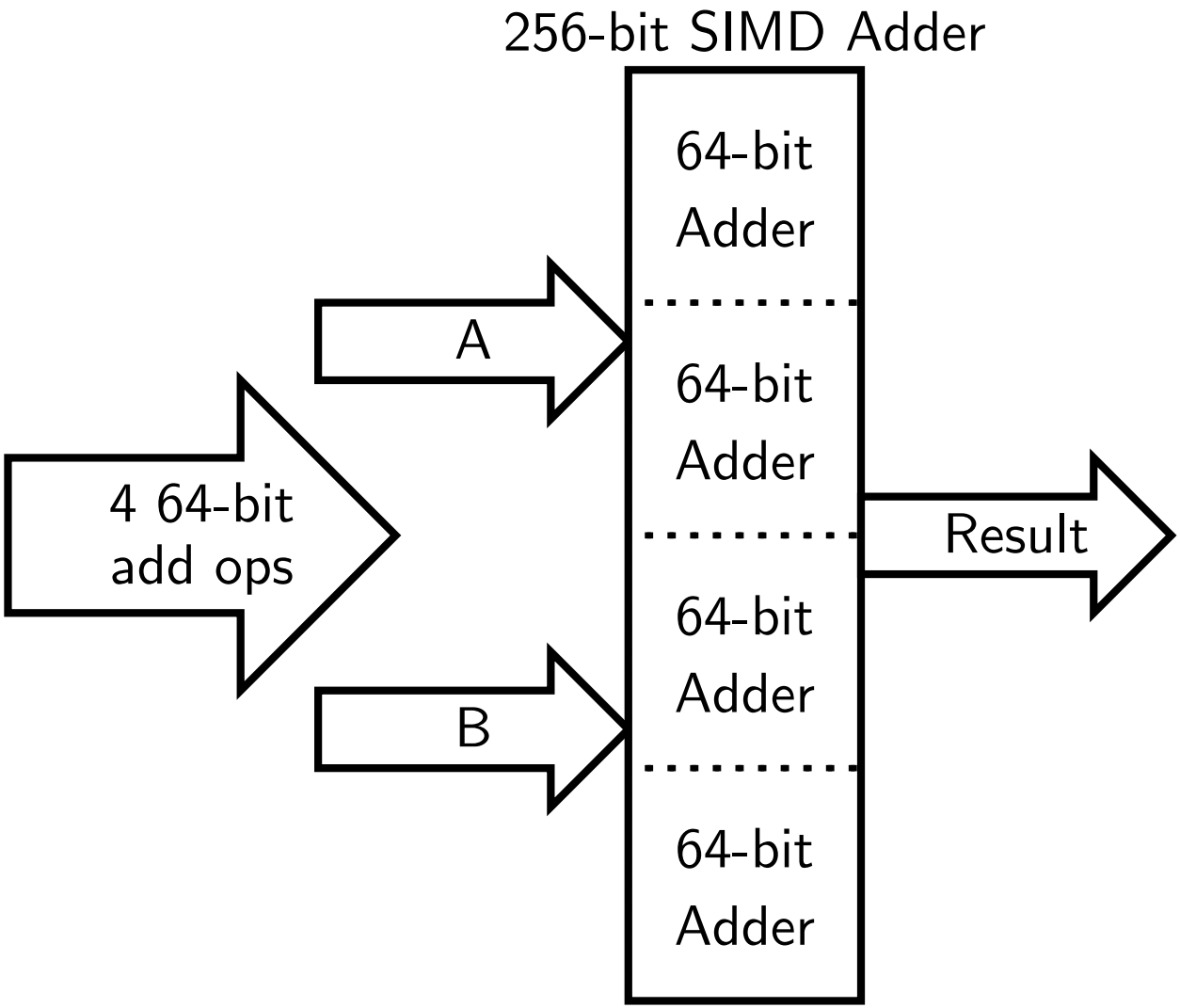


Big-Integer Addition on an example CPU

Disclaimer: SVP64 is designed for everything from tiny to big and fast CPUs, this example only shows a hypothetical big and fast CPU design

Big-Integer Addition on an example CPU



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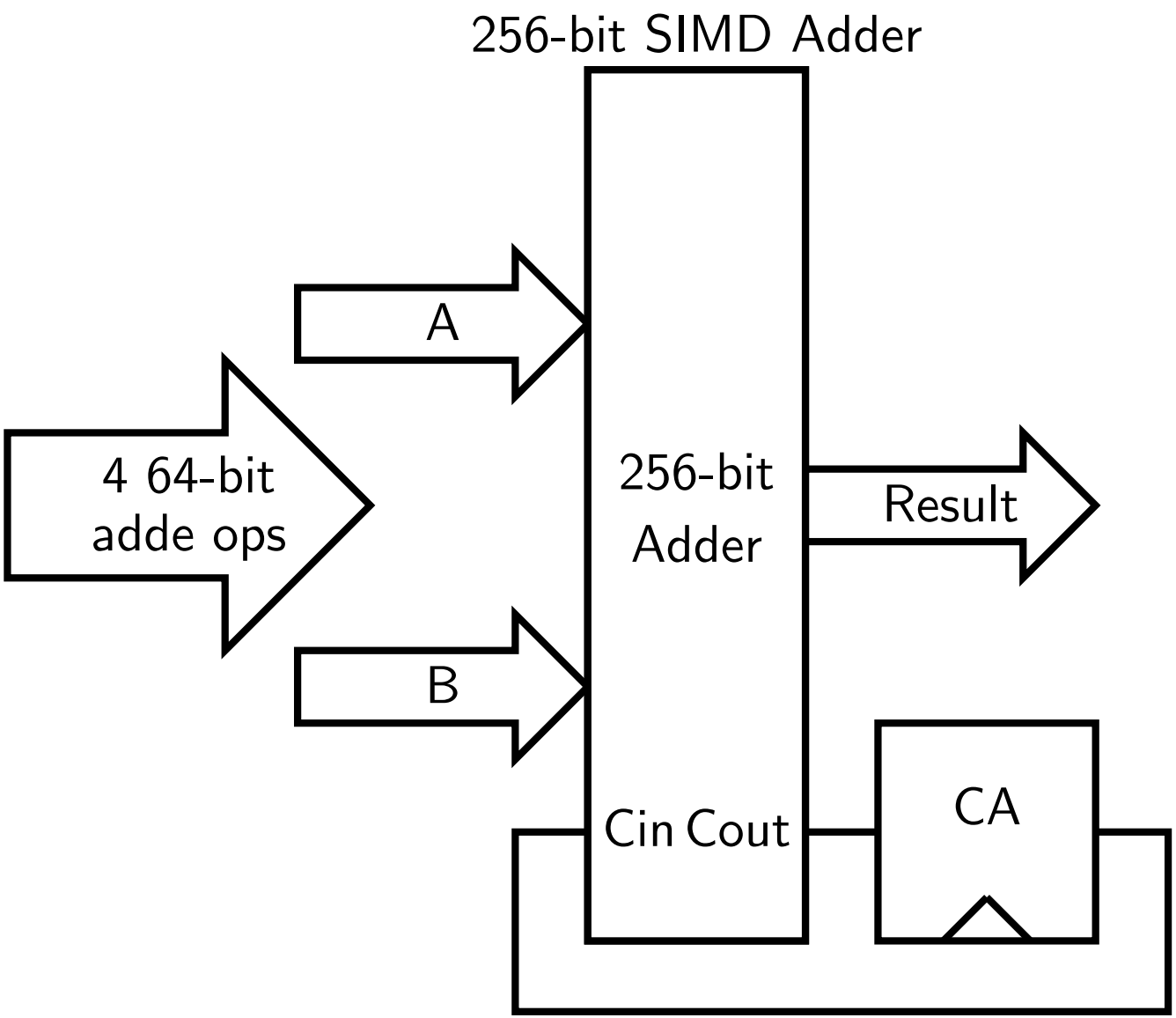

Big-Integer Multiply on SVP64

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- new instruction: `maddedu RT, RA, RB, RC`
- $64 \times 64 + 64 \rightarrow$ 128-bit Multiply-Add
- Semantics as used in this presentation (somewhat simplified):

```
result = (RA * RB) + RC
RT = LSB_HALF(result)
RC = MSB_HALF(result)
```

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```
# 64-bit input in r3
# 256-bit input in r20-23
# 320-bit output in r4-8
setvl 0, 0, 4, 0, 1, 1 # makes stuff run 4 times
li r8, 0  # clear carry register
sv.maddedu *r4, r3, *r20, r8  # carrying multiply
```

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setvl 0, 0, 4, 0, 1, 1 # makes stuff run 4 times
li r8, 0  # clear carry register
sv.maddedu *r4, r3, *r20, r8  # carrying multiply

# expands to:
li r8, 0
maddedu r4, r3, r20, r8
maddedu r5, r3, r21, r8
maddedu r6, r3, r22, r8
maddedu r7, r3, r23, r8
```
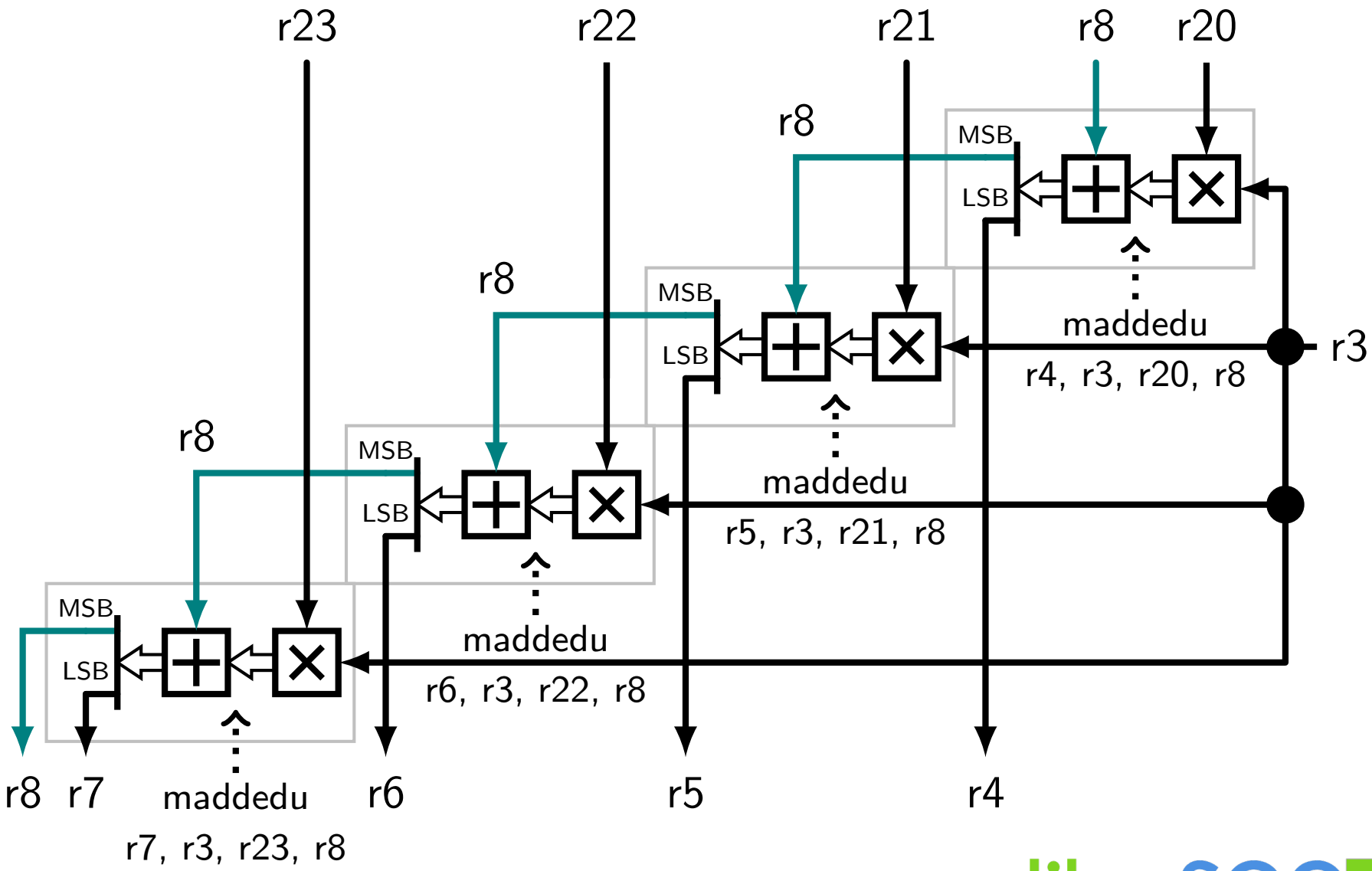
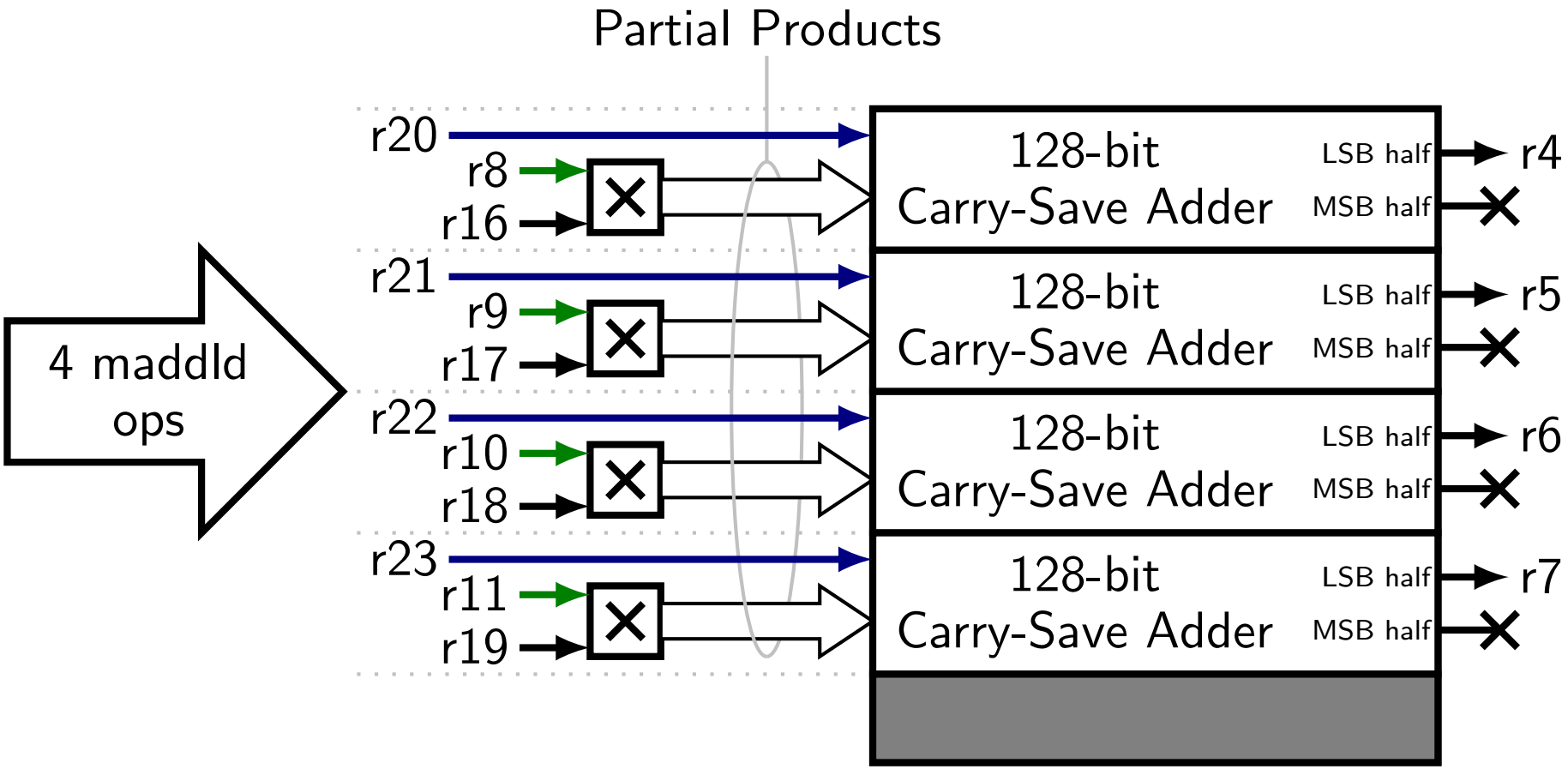

Big-Integer Multiply on SVP64



Big-Integer Multiply on an example CPU

```
sv.maddld *r4, *r8, *r16, *r20  # mul-add
```



Big-Integer Multiply on an example CPU

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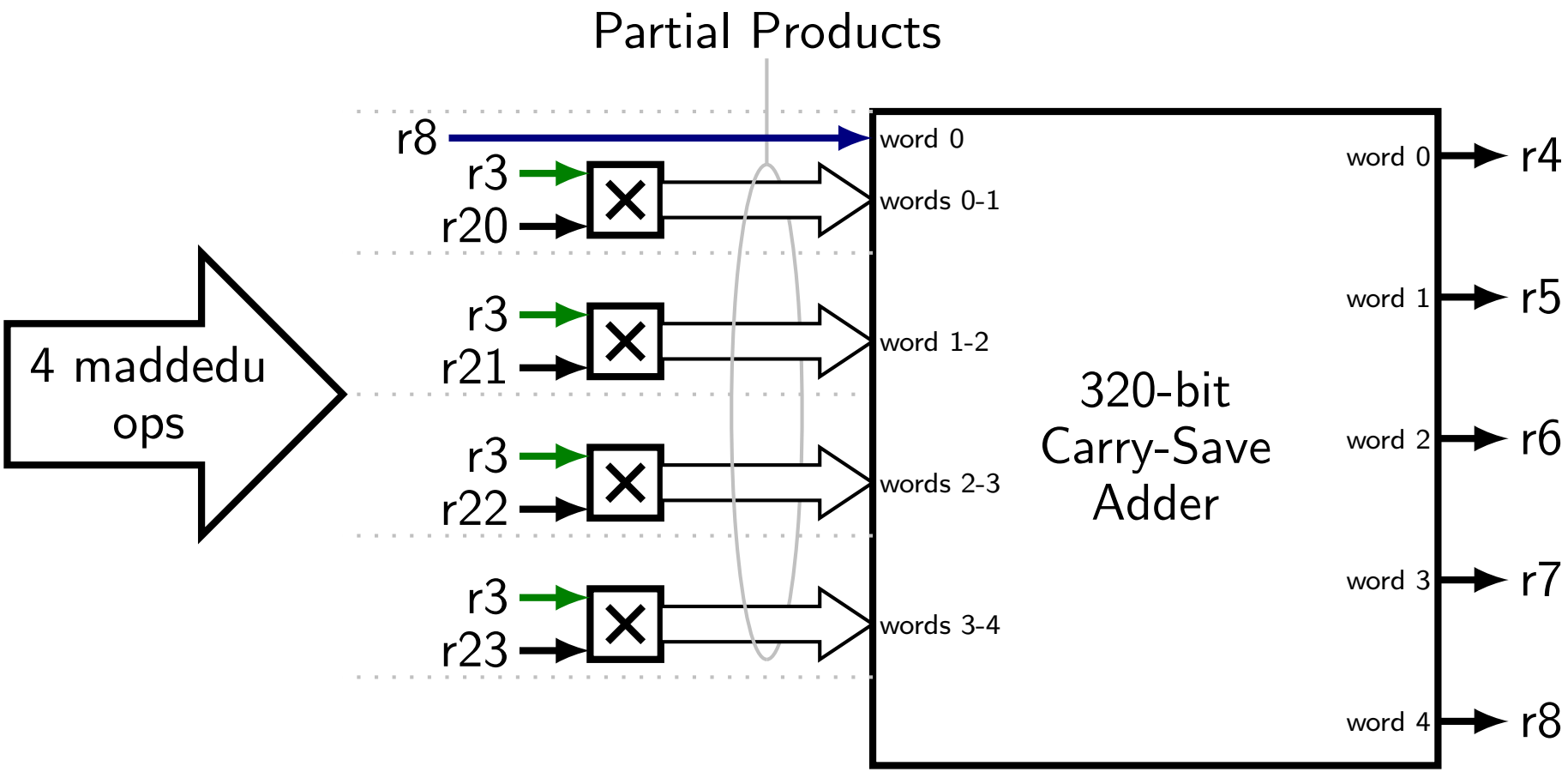

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